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APPLICATION FOR LETTERS PATENT

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INTEGRATED CIRCUIT MODULE HAVING ON-CHIP SURGE CAPACITORS

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application Serial Number 08/965,741, filed November 7, 1997, pending, which is a continuation of U.S. Patent Application Serial Number 08/671,248, filed June 27, 1996, now U.S. Patent 5,687,109, which is a continuation of U.S. Patent Application Serial Number 08/178,716, filed January 10, 1994, now abandoned, which is a continuation of U.S. Patent Application Serial Number 08/034,001, filed March 19, 1993, which is now U.S. Patent 5,307,309, which is a continuation of U.S. Patent Application Serial Number 07/774,121, filed October 8, 1991, abandoned, which is a continuation of U.S. Patent Application Serial Number 07/291,294, filed December 27, 1988, now abandoned, which is a continuation-in-part of U.S. Patent Application Serial Number 07/200,673, filed May 31, 1988, now abandoned.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: This invention relates to arrays of semiconductor circuit devices, in which a plurality of integrated circuit chips is mounted to a printed circuit board, or the like, for connection to a main circuit board (mother board). The invention is directed to power supply filtering of SIMM (single in-line memory module) arrays and similar arrays.

[0003] This invention further relates to semiconductor devices and, more specifically, to circuit connections on semiconductor devices and to the reduction of voltage transients on the semiconductor devices.

[0004] State of the Art: Integrated semiconductor devices are typically constructed en masse on a wafer of silicon or gallium arsenide. Each device generally takes the form of an integrated circuit (IC) die, which is attached to a lead frame with gold wires. As shown in Figure 1, the die and lead frame are then encapsulated in a plastic or ceramic package, which is then recognizable as an IC "chip". IC chips come in a variety of forms, such as dynamic random access memory (DRAM) chips, static random access memory (SRAM) chips, read only memory. (ROM) chips, gate arrays, and so forth. The chips are interconnected in myriad combinations on printed circuit boards by a number of techniques, such as socketing and soldering.

[0005] Interconnections among chips arrayed on printed circuit boards are typically made by conductive traces formed by photolithography and etching processes. Semiconductor circuit devices, including DRAMs, SRAMs and gate arrays, are essentially switching devices. As the output drivers within those chips create intermittent current flow on associated conductive traces, the traces behave as inductors, creating voltage surges which have the potential for creating logic errors. Other logic-damaging transient voltages, caused by voltage fluctuations at the power line and the interaction of other circuit components in the system, may also be present.

[0006] Semiconductor devices typically take the form of a semiconductor die. The semiconductor die 11 is generally attached to a lead frame 13 within a package, by means of fine gold wires 15, as shown in Figure 1. these fine gold wires function as lead frame connection wires. the lead frame and die assembly is then encapsulated, in the form of the familiar integrated circuit "chip". The packaged chip is then able to be installed on a circuit board by any number of techniques, such as socketing and soldering.

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[0007] In order to render innocuous the transient voltages which regularly appear in logic circuits, decoupling capacitors are commonly used as low-frequency bypass filters.

[0008] The gold connection wires, because of their length relative to their diameter, function as inductors. As current through the gold connection wires is alternately switched on and off, voltage spikes occur. In order to reduce the effects of voltage transients, external capacitors have been installed either within the semiconductor package or on a circuit board onto which the semiconductor packages are installed. In either case, the capacitor is on an opposite side of the lead frame connection wire from the semiconductor die. This establishes the circuit shown in Figure 2. This equivalent circuit represents an inappropriate arrangement for filtering voltage transients which would affect active circuit 11.

[0009] One circuit-board-mounted semiconductor chip array that is of particular interest is the SIMM (single in-line memory module). SIMM boards are typically constructed with such capacitors, which are usually located beneath or adjacent memory array circuit chips on the SIMM.

[0010] SIMM (single in-line memory module) boards are circuit arrays which consist of byte multiples of memory chips arranged on a printed circuit board or comparable mounting arrangement. The SIMM board is connected to a circuit control board by an edge connector.

[0011] The SIMM is a highly space-efficient memory board having no on board address circuitry and which is designed to plug directly into the address, data and power-supply buses of a computer so that the randomly-addressable memory cells of the SIMM can be addressed directly by the computer's CPU rather than by a bank-switching technique commonly used in larger memory expansion boards. Memory cells on the SIMM are perceived by the computer's CPU as being no different than memory cells found on the computer's mother board. Since SIMMs are typically populated with byte multiples of DRAMs, for any eight bit byte or sixteen bit byte or word of information stored within a SIMM, each of the component bits will be found on a separate chip and will be individually addressable by column and row. One edge of a SIMM module is a card-edge connector which plugs into a socket on the computer which is directly connected to the computer buses required for powering and addressing the memory on the SIMM.

[0012] The control board may be any of a number of circuits which address memory arrays. Examples include computer mother boards, daughter boards which plug into a mother board, wherein the daughter board functions as a mother board for the SIMM module, peripheral devices with a capability of using add-on memory, and special purpose equipment which uses memory. It is also possible to use small modules of arrays of similar circuits for purposes other than memory applications.

[0013] The capacitor on the SIMM, mounted external to the memory chips, establishes an inappropriate arrangement for filtering voltage transients. Therefore, it is desirable to provide capacitance on the other side of the inductor, i.e., the side of the inductor that the device is connected to.

[0014] Present SIMM boards are provided with surface-mounted decoupling capacitors, which cannot be seen in plan view. In the usual case, one decoupling capacitor is mounted beneath each DRAM chip, between bus voltage (V_{CC}) input and the connection to ground. The

V_{CC} bus and the ground-plane bus on the circuit board are not visible in a plan view since those particular bus traces are located between two of the board's six layers.

[0015] In most cases, each of the module's decoupling capacitors are connected in parallel between the V_{CC} bus and the ground plane bus. As long as the dielectric of each of the eight capacitors is intact, the module is functional. However, a short in any one of the eight capacitors will result in the V_{CC} buss becoming shorted to the ground-plane bus, whereupon the module will begin to draw an inordinate amount of current which will invariably result in its destruction.

[0016] Decoupling capacitors of the surface-mount type are particularly susceptible to shorting, since they have no leads to thermally isolate them as they are soldered to a circuit board with infrared energy at temperatures of up to 400°C (700°F). Even if a surface-mount capacitor survives the mechanical shock generated by the soldering process, it is still vulnerable to other types of mechanical stress. For example, by simply bending a SIMM having surface-mounted capacitors, the capacitors may be compromised. And, even if a SIMM passes testing (an indication that the decoupling capacitors are at least not shorted), it may have a relatively high failure rate when placed in use. SIMMs of the type shown in Figure 9 have an unacceptable average failure rate traceable to shorted decoupling capacitors during the first 90 days of use of roughly 3-10 per 100,000.

[0017] Single in-line packages (SIPs) are similar in design to SIMMs, except that instead of having a card edge-type connector, SIPs have pins which are either socketed or soldered for connection to a bus. The problems associated with the decoupling capacitor system of SIMMs also apply to SIPs.

[0018] Most semiconductors, including all DRAMS, include capacitors. For example, a 4 megabit DRAM includes over 4 million capacitors each. For the purpose of storing individual bits of information, these capacitors are accessed by connections through access transistors and sense amplifiers, connected through a peripheral circuit. The present invention concerns adding filter capacitance to such devices in order to provide protection from voltage transients which may not be afforded by what may be millions of other capacitors on the semiconductor device.

[0019] Semiconductor circuit devices are designed with an architecture which places their functional circuitry within a confined area, usually rectangularly shaped. At the perimeter (either outside or inside) of the rectangularly shaped area are a series of contact pads and a substantial amount of chip area which is occupied by conductor buses, but is unoccupied by active circuit devices. Unlike many of the circuit elements on a semiconductor circuit device, filter capacitors need not be built to precise specifications. It is, therefore, possible to utilize perimeter areas and portions of semiconductor chip areas which form major border areas between active portions of the semiconductor circuit device.

[0020] There is a significant advantage in providing that any added circuit elements be on the same side of a chip wafer as other circuit elements, because of manufacturing techniques and tolerances. Conventionally, semiconductor circuit devices are arrayed on one side of a die wafer. It would, therefore, be advantageous to design a filtering element which would not significantly expand the die area (chip area) required for each die.

[0021] There is a certain portion of the die area which is not particularly suitable for active circuitry. This includes chip area occupied by bus lines, which are normally metallization which overlays most or all of the patterned layers which make up the active circuitry on the die.

BRIEF SUMMARY OF THE INVENTION

[0022] In accordance with the present invention, capacitance filtering is provided for a circuit having an array of similar semiconductor circuit devices, such as a SIMM (single in-line memory module) array of semiconductor circuit devices. The semiconductor circuit devices are formed with capacitors located primarily in border areas, including perimeter border areas and intermediate border areas.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0023] Figure 1 shows a top view of a semiconductor device attached by pads to the lead frame;

[0024] Figure 2 shows an equivalent circuit of a semiconductor device connected to a lead wire and an off-chip capacitor;

[0025] Figure 3 shows an equivalent circuit of a semiconductor circuit device connected through a lead frame connection wire and having an on-chip decoupling capacitor;

[0026] Figure 4 shows a top view of a semiconductor device which incorporates a decoupling capacitor;

[0027] Figure 5 shows a top view of a semiconductor device, in which a decoupling capacitor is placed along an intermediate boundary area of the chip architecture;

[0028] Figures 6 and 7 show connection arrangements for N-channel and P-channel capacitors, respectively;

[0029] Figure 8 shows a cross-sectional view of an arrangement in which two capacitors are connected in series in order to increase breakdown voltage;

[0030] Figure 9 shows a SIMM module constructed in accordance with the present invention;

[0031] Figure 10 shows a parallel arrangement of capacitors on a memory array;

[0032] Figure 11 shows the use of a SIP board; and

[0033] Figure 12 shows a schematic block diagram representation of semiconductor circuit device having an on-chip regulator.

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DETAILED DESCRIPTION OF THE INVENTION

[0034] Referring to Figure 1, a semiconductor device includes a die 11 which is connected to a lead frame 13 by a plurality of lead wires 15. The lead wires 15 are attached to the die 11 at pads or contact points 17.

[0035] The lead wires 15 function as inductors 15′ and 15″, as schematically shown in Figures 2 and 3. While an external capacitor 21 is often provided, an appropriate filter capacitance would be located on the die side of the lead wire 15″, as schematically shown in Figure 3, at 23.

[0036] Figure 4 shows details of one end of the die 11 constructed with the present invention. A pair of capacitors is defined by an active area of the substrate 30 and a polysilicon (poly) layer which is formed into strips 25, 26. The active area of the substrate 30 is in electrical communication with a first bus line V_{SS}. The poly strips 25, 26 are in electrical communication

with a second bus line V_{CC}. Oxide is used to separate the strips 25, 26 from the active area of the substrate 30.

[0037] The capacitors defined by the strips 25, 26 are on a location of the die 11 which underlies VX and V_{CC}, as well as other buses 31. The buses 31 (including VX and V_{CC}) are typically metallization layers, and real estate occupied by the buses 31 cannot be used for most types of active circuitry. This is because active circuitry requires utilization of layers as outputs, which, in this case, is prevented by the buses 31 which are used for routing signals from the left end to the right end of the chip.

[0038] Figure 5 shows a configuration in which a pair of capacitors is defined by an active substrate area 55 along an intermediate portion of a semiconductor die 57. A plurality of poly strips 25-26, superimposed over the active poly area, defines a plurality of capacitors. Circuit buses 71 are superimposed over the capacitors formed by the poly strips so that the capacitors do not occupy real estate that could be used for most active circuit devices.

[0039] The invention has been described in terms of connection to circuit buses which have external connections. It is possible that an additional circuit may be placed between the bus and an external connection. A likely example of such an additional circuit would be a voltage regulating circuit. It is possible to connect the capacitor to a bus which extends between such an additional circuit and a main portion of the integrated circuit device.

[0040] The present embodiment contemplates the use of N channel capacitors, with V_{SS} connected to the active area of the substrate 30'x and V_{CC} connected to poly 75. This is shown in Figure 6. It is possible to construct P channel capacitors with V_{CC} connected to the active area of the substrate 30" and V_{SS} connected to poly 85. This is shown in Figure 7. Each of these is an enhancement mode capacitor, which has a preferential voltage polarity. It is also possible to form these capacitors as depletion mode capacitors.

[0041] It may also be the case that two capacitors may be connected in series in order to increase the total breakdown voltage of the combined capacitors. Enhancement mode capacitors require adjustment for their preferential voltage polarity. This can be accomplished through interconnects or similar means. Depletion mode capacitors, on the other hand, have less preferential voltage polarity. If the capacitors are not polarization sensitive, then the capacitors

can have a common poly plate 91 or a common active area 95, as schematically shown in Figure 8.

[0042] Figure 9 shows a SIMM (single in-line memory module) board 101, which consists of a printed circuit board 103, on which are mounted a plurality of semiconductor memory devices such as DRAMs 105. The printed circuit board 103 includes an edge connector 107, which extends from the printed circuit board 103 in order to permit the SIMM board 101 to be plugged into a computer bus (not shown) on a computer. The computer bus has a capability of addressing the DRAMs 105 on the board in predetermined sequence, as defined by the SIMM protocol. Typically, an entire row of DRAMs 105 is simultaneously addressed to obtain a byte of information. Other addressing schemes are, of course, possible.

[0043] Figures 10 and 11 show the use of capacitors on DRAMS 105. A SIP (single in-line package) board 111, as shown in Figure 11 and similar boards, which use a connector to connect an array of similar components with parallel address circuitry through a connector may also be used with the invention..

[0044] By providing a capacitor as a part of the individual DRAMs 105, the SIMM board 101 does not have to be constructed with discrete capacitors mounted to the board. As mentioned, having a capacitor on the die serves to filter the effects of lead wire inductance. Further, since the SIMM board includes byte multiples of DRAMs, the capacitors on board each chip are connected in parallel. While this does not increase the capacitance on the die side of the lead wires, the total capacitance is thereby increased, with the added benefit that some capacitance is on the die side of the lead wire of each chip.

[0045] The elimination of discrete capacitors further eliminates a failure mode. It has been found that as many as one in 10,000 discrete capacitors has failed subsequent to burn-in. This has resulted in an added field failure rate of close to one in 1000 for an 8 or 9 device part. Eliminating the discrete capacitors is believed to significantly reduce this failure rate.

[0046] There is a possibility that the impedance of the multiple rows of the DRAMs 105 results in a mismatch (of impedance) of multiplexed RAS and CAS signal lines if the signals are intended for use with a single row of DRAMs. In order to cause the impedance to match that of inputs, termination capacitors (not shown) may be are used to compensate for the

shifted impedance load of the DRAMs caused by the multiple rows of DRAMs 105. The termination capacitors may be discrete elements, even if load capacitors are incorporated onto the DRAMs 105.

[0047] Referring to Figure 12, a regulator 98 is on-chip with capacitor 23 and die 11.

[0048] What has been described is a specific embodiment of the invention. The invention is expected to be able to work with other memory devices, such as SRAMS and VRAMS. It is anticipated that variations can be made on the preferred embodiment and, therefore, the invention should be read as limited only by the claims.